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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/039,010
Filing Date: December 31, 2001
Appellant(s): OLARIG ET AL.

Jeffrey R. Peterson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed September 22, 2008 appealing from the Office action mailed November 27, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,405,286	Gupta	07-2001
5,761,726	Guttag	06-1998
6,272,577	Leung	10-1997
5,737,575	Blaner	4-1998
6,230,225	Olarig	12-1998
5,864,712	Carmichael	01-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8-11, 13, 16-18, 20-23, 25-27 and 29 are rejected under 35 U.S.C 103(a) as being unpatentable over Leung et al. (US 6,272,577) in view of Guttag (5,761,726).

As per claim 1, Leung et al. discloses a method for transacting between an initiator device and a plurality of target devices [*a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65]; sending a multicast transaction from the initiator device to the plurality of target devices, wherein sending the multicast transaction comprises sending a multicast transaction to the single base address associated with each of the plurality of target devices [*a base address which identifies the memory module*; col.10, lines 20-23; *the memory modules are equipped with independent address and command decoders so that they function as independent units, each with their own base address; the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access*; col.5, lines 5-8; col.4, lines 31-33; *multiple bank operations such as broadcast-write and interleaved access possible; a memory device able to handle a broadcast write operations simultaneously*; col.5, lines 27-31]; executing the transaction when the transaction is received by the plurality of target devices according to the configuration of the target devices [*since each memory module is a complete functional unit, the memory module architectures allows parallel processes and multiple memory module operations to be performed within different memory modules*; col.4, lines 42-45].

Leung does not explicitly teach associating each of the plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices as recited in the claim.

Guttag, however, discloses associating each of the plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices [col. 5, lines 36-41; col.172, lines 48-55] to generate addresses for read/write access to data stored within a plurality of memories (col. 5, ll 40-45).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Leung to include associating each of the plurality of target devices with a single base address, wherein the same single base address is associated with each of the plurality of target devices because doing so would have generated addresses for read/write access to data stored within a plurality of memories (col. 5, ll 40-45) as taught by Guttag.

As per claim 2, Leung et al. discloses assigning a base memory address to be shared by the plurality of target devices [*a base address which identifies the memory module*; col.10, lines 20-23; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65]; and assigning a first portion of memory to a first target device of the plurality of target devices [*each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract].

As per claim 3, Leung et al. discloses the transaction is a read request for a block of stored data from memory [*a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27; *the address information comprises a base address of the memory device to be accessed*; col.31, lines 12-14]; recognizing the base memory address from the read request *[each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract *; the memory modules are equipped with independent address and command decoders so that they function as independent units, each with their own base address*; col.4, lines 31-33]; initiating a read operation by the plurality of target devices assigned to the base memory address [*each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract; *a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27; *a base address which identifies the memory module*; col.10, lines 20-23]; fetching stored data from a portion of memory associated with each of the target devices, the data being concurrently fetched by each associated target device and sending the fetched data to the initiator device [*another multiple-array operation is an interleaved burst operation, in which a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27].

As per claim 4, Leung et al. discloses, the transaction is a write request for data to be stored in memory [*a read or write command causes data to be read or written to different*

arrays in a time multiplexed data burst; col.24, lines 23-27]; recognizing the base memory address from the write request [*address information comprises a base address of the memory device to be accessed*; col.31, lines 13-14; *a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27]; initiating a write operation by the plurality of target devices assigned to the base memory address [*each memory module has independent address and command decoders to enable independent operation so that each memory module is activated only when a memory access operation is performed*; abstract; *a base address which identifies the memory module*; col.10, lines 20-23]; and writing data of the write request to a portion of memory associated with each target device, the data being concurrently written by each associated target device[*another multiple-array operation is an interleaved burst operation, in which a read or write command causes data to be read or written to different arrays in a time multiplexed data burst*; col.24, lines 23-27].

As per claim 5, Leung et al. discloses, wherein the target devices comprise input/output Controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 6, Leung et al. discloses, the target devices comprise disk array controllers [Fig. 19; *controller 1920*].

As per claim 8, Leung et al. discloses, a plurality of target groups [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 9, the rationale in the rejection of claim 1 is herein incorporated. Leung et al. further discloses, a method for transacting data stored in memory between an initiator device and detecting a multicast transaction request [*multiple bank operations such as broadcast-write and interleaved access possible; a memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously*; col.5, lines 27-31]; accessing a first portion of memory by a first target device associated with the first portion of memory in response to the multicast transaction request [col. 4, lines 30-46; col. 5, lines 21-31; col.19, lines 42-47]; accessing a second portion of memory by a second target device associated with the second portion of memory concurrently with access to the first portion of memory in response to the multicast transaction request wherein the first and second portions of memory are accessed with a single base address associated with the first target device and the second target device [col. 4, lines 30-46; col. 5, lines 21-31; *a first field contains a base address which identifies the memory module;* col.10, lines 21-25; *the present invention groups at least two memory arrays or banks into a memory module*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module*; col.5, lines 5-8].

As per claim 10, Leung et al. discloses, the target devices comprise input/output Controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 11, Leung et al. discloses, the target devices comprise disk array Controllers [Fig. 19; *controller 1920*].

As per claim 13, Leung et al. discloses accessing a plurality of target devices, wherein the plurality of target devices are divided into a plurality of groups, wherein each of the plurality of groups is associated with a single base memory address configured to address the target devices within that group [*the present invention groups at least two memory arrays or banks into a memory module*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory*; col.5, lines 5-8].

As per claim 16, the rationale in the rejection of claim 1 is herein incorporated. Leung et al. further discloses, a computer system comprising a bus [*memory device and allowing each memory module to have a communication address on the I/O bus system*; col.4, lines 54-56]; an initiator device coupled to the communications bus for initiating a transaction request [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46]; and a plurality of target devices coupled to the communications for executing the transaction request, the plurality of target devices executing the transaction request by each target device concurrently responding to a portion of the transaction request, wherein the initiator device is configured to multicast a transaction request to the plurality of target devices using a single base address associated with the plurality of target devices [*a first field contains a base address which identifies the memory module by communication address. A second field contains an address which identifies the memory array within the memory module*. col.10, lines 21-25; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65; *a memory device in accordance with the present invention provides multiple commands, one after*

another, to different arrays; col.25, lines 15-17; *a base address which identifies the memory module*; col.10, lines 20-23; *the memory modules are equipped with independent address and command decoders so that they function as independent units, each with their own base address*; *the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 17, Leung et al. discloses the target device comprises input/output controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 18, Leung et al. discloses a target device comprises disk array controllers [Fig. 19; *controller 1920*].

As per claim 20, Leung et al. discloses the plurality of target devices comprise a target group [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 21, Leung et al. discloses a plurality of target groups [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24].

As per claim 22, Leung et al. discloses the transaction is a multicast read request [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*;

col.7, lines 45-46; *when a memory read or write command is decoded, each memory module examines the communication ID of the command*; col.19, lines 42-47].

As per claim 23, Leung et al. discloses the transaction is a multicast write request [*multiple bank operations such as broadcast-write and interleaved-access*; col.5, lines 27-29; *a memory device in which a single input data stream can be simultaneously written to multiple memory arrays*; col.3, lines 63-65].

As per claim 25, the rationale in the rejection of claim 1 is herein incorporated. Leung et al. further discloses a computer system comprising a processor, a bus coupled to the processor [*the two processors can reside on the same bus using the same memory module*; col.10, lines 40-42]; an initiator device coupled to the bus for issuing a multicast transaction, and a plurality of target devices coupled to the bus for executing the multicast transaction with concurrent data responses from a plurality of interleaved memory regions, wherein the initiator device is configured to multicast the transaction request to the plurality of target devices using a single base address associated with the plurality of target devices [*all memory transactions are initiated by either I/O module 104 or by devices connected to I/O bus 106*; col.7, lines 45-46; *multiple bank operations such as broadcast-write and interleaved access possible. A memory device able to handle a broadcast write bandwidth of 36 gigabytes per second and 36 memory operations simultaneously*; col.5, lines 27-31; *a first field contains a base address which identifies the memory module by communication address;* col.10, lines 21-25; *the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *in each memory module, a*

programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access; col.5, lines 5-8].

As per claim 26, Leung et al. discloses the target devices comprise input/output controllers [*I/O module 104 contains a controller*; col.7, lines 46-47].

As per claim 27, Leung et al. discloses the target devices comprise disk array Controllers [Fig. 19].

As per claim 29, Leung et al. discloses a plurality of target devices are divided into a plurality of target groups, wherein each of the target groups is associated with its own base address [*the present invention groups at least two memory arrays or banks into a memory module and connects all the memory modules to a bus*; col.4, lines 20-24; *in each memory module, a programmable identification register contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access*; col.5, lines 5-8].

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leung in view of Guttag (5,761,726) and further in view of Carmichael et al. (US 5,864,712).

As per claim 24, Leung and Guttag disclose the claimed invention as detailed above in the previous paragraphs.

Leung and Guttag do not explicitly teach the communications bus comprises a Peripheral Component Interconnect (PCI) bus as recited in the claim.

However, Carmichael discloses the bus comprises a Peripheral Component Interconnect (PCI) bus [*the bridge 36 may simply provide an extension of the processor's bus, or may buffer and extend the processor bus using an entirely different bus structure and protocol such as PCI*; col.6, lines 46-50].

Thus it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Leung and Guttag to include a PCI bus because doing so would have provided an extension of the processor's bus and to buffer and extend the processor (col.6, lines 46-50) as taught by Carmichael.

Claims 32 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guttag 5,761,726) Gupta (6,405,286) in view of Blaner (5,737,575).

As per claim 32, Guttag discloses a plurality of devices having a common base address and a transaction request directed to the common base address [*a plurality of corresponding memories having a unique addressable memory of a single memory space wherein these corresponding memories have a corresponding base address within the single memory address space;* col. 5, lines 36-41]. It is worth mentioning that Guttag discloses a one to one correspondence between the "plurality of memories" and the "**a** corresponding fixed base address".

Guttag does not explicitly disclose a computer comprising a memory; a controller configured to logically divide the memory into a plurality of interleaved memory regions;

and a plurality of devices, wherein each of the plurality of devices is associated with one of the interleaved memory regions and wherein each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction request.

However, Gupta discloses a computer comprising a memory [col.1, lines 24-25]; a controller configured to logically divide the memory into a plurality of interleaved memory regions [Fig.2]; and a plurality of devices, wherein each of the plurality of devices is associated with one of the interleaved memory regions and wherein each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction request [col.6, lines 21-28; col. 16, ll 12-24]. Gupta further discloses each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction requests [*two or more memory busses can each perform memory transactions simultaneously, with each memory bus coupled to one or more memory bus segments, wherein a single memory transaction can be active on a single memory bus segment at any given time, and each memory bus segment is coupled to one or more interleaved memory banks*; col. 16, ll 15-23].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system og Guttag to include a computer comprising a memory; a controller configured to logically divide the memory into a plurality of interleaved memory regions; and a plurality of devices, wherein each of the plurality of devices is associated with one of the interleaved memory regions and wherein each of the devices simultaneously accesses its associated interleaved memory region in

response to a single transaction request so that multiple CPUs tend not access the same memory bank at the same time (col. 6, lines 23-26] as taught by Gupta.

Guttag and Gupta do not explicitly disclose each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction requests.

However, Blaner discloses each of the devices simultaneously accesses its associated interleaved memory region in response to a single transaction requests [*interleaved memory banks wherein a group of the interleaved memory banks are accessible in parallel in response to a single access*; col. 8, ll 22-26].

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Guttag and Gupta in view of Blaner to include devices each simultaneously accessing its associated interleaved memory region in response to a single transaction requests because this would have allowed simultaneous access to multiple pages of memory and reduced latency (col. 2, ll 65-67) as taught by Blaner.

As per claim 47, Guttag discloses a method of performing operations accessing memory comprising assigning a common base address to a plurality of disk drives to create a collective target group [col. 172, ll 48-60; col. 5, lines 36-41].

Guttag, however, does not explicitly disclose assigning a portion of data storage to each disk drive of the collective target group.

Gupta discloses assigning a portion of data storage to each disk drive of the collective target group [Figs. 1-2; col. 1, lines 37-64; *memory array with multiple banks of rows and columns divided into different arrays of memory or banks that can operate independently*; col. 2, lines 55-60]; initiating a memory operation to the collective target group using a common base address [col. 16, ll 15-23]; wherein each disk drive recognizes the common base address and simultaneously and simultaneously executes the memory operation on the portion of data storage to which the disk drive is assigned [col. 16, lines 15-23].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system of Guttag to include assigning a portion of data storage to each disk drive of the collective target group so that multiple CPUs tend not access the same memory bank at the same time (col. 6, lines 23-26] as shown in Gupta.

However, Guttag and Gupta do not explicitly disclose initiating the memory operation as an interleaved operation and as a single request to the collective target group.

Blaner discloses initiating the memory operation as an interleaved operation and as a single request to the collective target group [*interleaved memory banks wherein a group of the interleaved memory banks are accessible in parallel in response to a single access*; col. 8, ll 22-26].

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant, to modify the system of Guttag and Gupta to include initiating the

memory operation as an interleaved operation and as a single request to the collective target group because doing so would have allowed simultaneous access to multiple pages of memory and reduce latency (col. 2, ll 65-67) as shown in Blaner.

Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over Guttag 5,761,726) Gupta (6,405,286) in view of Blaner (5,737,575) and further in view of Olarig (6,230,225).

As per claim 48, Guttag, Gupta, and Blaner do not explicitly disclose initiating an interleaved memory operation as a single request comprises initiating a multicast transaction from a SCUSI controller over a multicast bus.

Olarig, however, discloses initiating an interleaved memory operation as a single request comprises initiating a multicast transaction from a SCUSI controller over a multicast bus [Fig.1, col. 1, lines 26-51].

Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system of Guttag, Gupta and Blaner to include initiating an interleaved memory operation as a single request which comprises initiating a multicast transaction from a SCUSI controller over a multicast bus because doing so would have facilitated broadcasting a single bus transaction to multiple targets (col.1, lines 5-10) as taught by Olarig.

Claims 33-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. (US 6,272,577) in view of Guttag (5,761,726) and further in view of Gupta (6,405,286).

As per claim 33, the rationale in the rejection of claim 1 is herein incorporated. Leung and Gutttag do not explicitly teach a method comprising dividing a section of memory into a plurality of interleaved memory regions as required by the claim.

Gupta, however, discloses a method comprising dividing a section of memory into a plurality of interleaved memory regions [col.6, lines 20-24].

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Leung Guttag to include dividing a section of memory into a plurality of interleaved memory regions because doing so would have allowed multiple CPUs not to tend accessing the same memory bank at the same time (col.6, ll 23-26) as taught by Gupta.

AS per claim 34, Gupta discloses executing the memory access comprises executing a read operation [col.6, lines 24-27].

As per claim 35, Gupta discloses executing the memory access comprises executing a write operation [col.6, lines 24-27].

As per claim 36, the rationale in the rejection of claim 1 is herein incorporated. Gupta further discloses a tangible machine readable medium comprising code to initialize a plurality of devices [col.11, lines 36-39]; and code to associate the single base address with a plurality of interleaved memory regions [col.6, lines 21-23]; col.12, lines 44-55].

Thus, it would have been obvious to combine Leung, Guttag, and Gupta for the same reasons shown above.

As per claim 37, Gupta discloses code to issue a single read command comprising the single base address [col.6, lines 11-14; col.4, lines 31-34; col.6, lines 53-54]; code to recognize the single base address as associated with the plurality of devices [col.10, lines 20-23; col.6, lines 53-54]; code to simultaneously execute a plurality of memory requests involving the plurality of devices [col.6, lines 21-28; col.6, lines 53-54]; code to receive data from the plurality of devices [col.8, lines 11-12; col.6, lines 53-55]; and code to write the received data to a bus [col.8, lines 14-16].

Thus, it would have been obvious to combine Leung, Guttag, and Gupta for the same reasons shown above.

As per claim 38, Gupta discloses code to issue a write command comprising the single base address [col.6, lines 12-15; col.4, lines 31-34; col.6, lines 53-56]; code to recognize the base address as associated with the plurality of devices [col.4, lines 31-

34; col.6, lines 53-56]; and code to simultaneously write to the plurality of devices [col.6, lines 21-28].

Thus, it would have been obvious to combine Leung, Guttag, and Gupta for the same reasons shown above.

Claims 39-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al. (US 6,272,577) in view of Guttag (5,761,726) and further in view of Olarig (6,230,225).

As per claim 39, Leung and Guttag do not explicitly disclose the multicast transaction comprises sending the multicast transaction from a disk controller to a plurality of disk drives.

Olarig, however, discloses the multicast transaction comprises sending the multicast transaction from a disk controller to a plurality of disk drives [Fig.1, *PCI device 150A, PCI Bridge 130, Memory 180*].

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant, to modify the system of Leung and Guttag to include sending multicast transaction to a plurality of disk drives because doing so would have enabled broadcasting of a single bus transaction to multiple target devices (col.1, lines 5-10) as taught by Olarig.

As per claims 40-41, and 43-44, Olarig discloses sending the multicast transaction comprises sending the multicast transaction from a SCSI controller to a plurality of SCSI devices [Fig.1, col.1, lines 26-51].

Thus, it would have been obvious to combine Leung, Guttag, and Olarig for the same reasons shown above.

As per claim 42, Olarig discloses the plurality of target devices comprises a plurality of disk drives [Fig.1, memory 180-190].

Thus, it would have been obvious to combine Leung, Guttag, and Olarig for the same reasons shown above.

Claims 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guttag 5,761,726), Gupta (US 6,405,286), in view of Blaner (5,737,575) and further in view of Olarig (6,230,225).

As per claims 45-46, Guttag, Gupta and Blaner disclose the claimed invention as discussed above with respect to claim 32. However, Guttag, Gupta and Blaner do not explicitly disclose sending the multicast transaction comprises sending the multicast transaction from a SCSI controller to a plurality of SCSI devices.

Olarig discloses sending the multicast transaction comprises sending the multicast transaction from a SCSI controller to a plurality of SCSI devices [Fig.1, col.1, lines 26-51].

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant, to modify the system of Guttag, Gupta, and Blaner to include sending the multicast transaction comprises sending the multicast transaction from a SCSI controller to a plurality of SCSI devices because doing so would have enabled broadcasting of a single bus transaction to multiple target devices (col.1, lines 5-10) as taught by Olarig.

(10) Response to Argument

Applicant argues on page 15, paragraph 2, that Leung and Guttag fail to disclose "sending a multicast transaction from an initiator device to a plurality of target devices" and "the same single address being associated with each of the plurality of targets" recited in claim 1.

The combination of Leung and Guttag was relied upon in rejecting the claims. Leung discloses [*a memory device which can be configured to simultaneously write data to multiple modules (i.e., multicast),* Abstract; *all memory transactions are initiated by I/O module 104*; col. 7, lines 45-46; *multiple bank operations such as broadcast-write and interleaved access possible; a memory device able to handle a broadcast write operations simultaneously*; col.5, lines 27-31; *since each memory module is a complete functional unit, the memory module architectures allows parallel processes and multiple memory module operations to be performed within different memory modules*; col.4, lines 42-45].

Guttag discloses "each of a plurality of n processors has a predetermined plurality of corresponding memories, wherein the predetermined plurality of memories have a corresponding fixed base address; and a base address

instruction executing on any one of the plurality of n processors generating the base address of the predetermined plurality of memories corresponding to the one processor; col. 172, ll 48-60". Furthermore, in col. 5, lines 36-41, Guttag discloses "a plurality of corresponding memories having a unique addressable memory of a single memory space wherein these corresponding memories have a corresponding base address within the single memory address space".

It is worth mentioning that Guttag discloses a one to one correspondence between the "plurality of memories" and the "**a** corresponding fixed base address".

Leung also discloses associating the plurality of target devices with a single base memory address [col.4, lines 31-34]; and executing a memory access using the single base memory address [col.4, lines 44-46]. Furthermore, Leung discloses the "single base memory" address claimed by Applicant [col.4, lines 30-35] where the base address can be associated with either a single target device or a group of target devices.

Appellant submits on page 17, paragraph of the remarks that Guttag does not disclose "a plurality of target devices with a single base address wherein the same single base address is associated with each of the plurality of target devices" recited in claim 1.

The combination of Leung and Guttag was relied upon in rejecting the claims. Guttag discloses "each of a plurality of n processors has a predetermined

plurality of corresponding memories, wherein the predetermined plurality of memories have a corresponding fixed base address; and a base address instruction executing on any one of the plurality of n processors generating the base address of the predetermined plurality of memories corresponding to the one processor; col. 172, ll 48-60". Furthermore, in col. 5, lines 36-41, Guttag discloses "a plurality of corresponding memories having a unique addressable memory of a single memory space wherein these corresponding memories have a corresponding base address within the single memory address space".

It is worth mentioning that Guttag discloses a one to one correspondence between the "plurality of memories" and the "**a** corresponding fixed base address".

Appellant argues on page 18, paragraph 2, that Leung and Guttag do not disclose "wherein sending the multicast transaction comprises sending a multicast transaction to the single base address associated with each of the plurality of target devices".

The combination of Leung and Guttag was relied upon in rejecting the claims. Guttag discloses "each of a plurality of n processors has a predetermined plurality of corresponding memories, wherein the predetermined plurality of memories have a corresponding fixed base address; and a base address instruction executing on any one of the plurality of n processors generating the base address of the predetermined plurality of memories corresponding to the

one processor; col. 172, ll 48-60", while Leung discloses associating the plurality of target devices with a single base memory address [col.4, lines 31-34]; and executing a memory access using the single base memory address [col.4, lines 44-46]. Furthermore, Leung discloses the "single base memory" address as claimed by Applicant [col.4, lines 30-35] where the base address can be associated with either a single target device or a group of target devices.

Appellant argues on page 19, paragraph 2 of the remarks that Leung fails to disclose "assigning a base memory address to be shared by the plurality of target devices" recited in claim 2.

The combination of Leung and Guttag was relied upon in rejecting the claims. Guttag discloses "wherein the predetermined plurality of memories have a corresponding fixed base address; and a base address instruction executing on any one of the plurality of n processors generating **the** base address of the predetermined plurality of memories; col. 172, ll 48-60".

Leung further discloses associating the plurality of target devices with a single base memory address [col.4, lines 31-34]; and executing a memory access using the single base memory address [col.4, lines 44-46]. Furthermore, Leung discloses the "single base memory" address as claimed by Applicant [col.4, lines 30-35] where the base address can be associated with either a single target device or a group of target devices.

Appellant submits that “the subject matter of claims 3 and 4 is not made obvious under Section 103 in view of Leung when taken alone or in combination with Guttag”.

Examiner respectfully disagrees. Regarding the limitations “the data being concurrently fetched by each associated target device” and “the data being concurrently written by each associated target device”, Leung discloses [“the memory device can be configured to simultaneously write data to multiple memory modules; Abstract; data can be simultaneously written to multiple memory arrays; col. 3, lines 63-67; the memory module architecture allows parallel accesses; col. 4, lines 42-45". Thus, claims 3 and 4 remain rejected under 35 U.S.C. 103 as shown in the rejection section above.

Appellant argues on page 20, paragraph 2, with respect to claims 1, 5, and 6, that "Examiner cited to the memory modules of Leung as being target devices and cited to the I/O module 104 and the controller 1920 as being target devices” and later concludes that “Examiner is inconsistently treating the references as well as the claims and this is improper and does not reflect an interpretation that one of ordinary skill in the art would give”.

Examiner respectfully disagrees. The recitations of “target devices” in claim 1 connote both the idea of having “target devices" of the same type (e.g., plurality of memory modules, **or** I/O controllers, **or** disk array controllers) and the idea that the "target devices" are of different kind (e.g., memory module/s, I/O controller/s, **and** disk array controller/s). It appears that Appellant misunderstood

the Examiner's position when it comes to the rejection of claims 5 and 6. Claims 5 and 6, to further limit independent claim 1, recite that the target devices **comprise** input/output controllers or disk array controllers. Note that claims 5 and 6 do not recite that the target devices ***are*** input/output controllers or disk array controllers but "the target devices" **comprise** input/output controllers or disk array controllers. As claimed, claims 5 and 6 do not prevent "the target devices" of claim 1 from being of one type (e.g., the memory modules of Leung) and of a different kind (e.g., input/output controllers and disk array controllers). In view of the foregoing, Leung discloses both "the plurality of target devices" of claim 1 [*plurality of memory arrays*; Fig. 1; col. 3, lines 63-65], and "the target devices comprise input/output controllers and disk array controllers" of claims 5 and 6 [*Fig. 1 shows I/O module 104 which controls the memory devices where one or more master devices can be attached to the I/O bus to control the operations in the system, and Fig. 19 shows a memory controller as that master device; note that Leung discloses one or more master devices control the operation of the system and the master device/s is/are in fact controller/s; hence, one more master devices here mean one or more controllers*; *thus, the plurality of controllers of Leung read on the claims 5 and 6 as the plurality of target devices*; col. 25, lines 28-38].

Appellant argues on page 20, paragraph 3 of the remarks that Leung fails to disclose "a plurality of I/O modules 104 or a plurality of controller 1920".

Examiner respectfully disagrees. Leung discloses [*Fig. 1 shows I/O module 104 which controls the memory devices where one or more master devices can be attached to*

the I/O bus to control the operations in the system and Fig. 19 shows a memory controller as that master device; col. 25, lines 28-38].

Appellant argues on page 21 of the remarks that Leung does not disclose "a plurality of target groups" recited in claim 8.

Leung discloses ["the memory device can be configured to simultaneously write data to multiple memory modules; Abstract; data can be simultaneously to multiple memory arrays; col. 3, lines 63-67. Leung further discloses the "single base memory" address as claimed by Applicant [col.4, lines 30-35] where the base address can be associated with either a single target device or a group of target devices.

Appellant argues on pages 21-23, that Leung and Guttag fail to disclose "accessing a first portion of memory by a first target device; accessing a second portion of memory by a second target device concurrently; the first and second portions of memory are accessed with a single base address associated with both the first target device and the second target device, wherein the first target device and the second target device are associated with the same single base address".

The reasoning above with respect to claim 1 applies to claim 9 as well.

Contrary to appellant's assumption, Examiner could not find any inconsistency in the rejection of claims 1 and 9.

The combination of Leung and Guttag was relied upon in rejecting the claims. Guttag discloses "each of a plurality of n processors has a predetermined plurality of corresponding memories, wherein the predetermined plurality of memories having a corresponding fixed base address; and a base address instruction executing on any one of the plurality of n processors generating the base address of the predetermined plurality of memories; col. 172, ll 48-60".

Leung discloses "associating the plurality of target devices with a single base memory address [col.4, lines 31-34]; and executing a memory access using the single base memory address [col.4, lines 44-46]. Furthermore, Leung discloses the "single base memory" address as claimed by Applicant [col.4, lines 30-35] where the base address can be associated with either a single target device or a group of target devices. Leung also discloses [*multiple bank operations such as broadcast-write are possible; a memory device able to handle a broadcast write 36 memory operations simultaneously*; col.5, lines 27-31; *a first field contains a base address which identifies the memory module by communication address. A second field contains an address which identifies the memory array within the memory module*. col.10, lines 21-25].

Appellant argues on page 24, with respect to claims 10 and 11, that "Examiner has inconsistently treated the claim term target device". Appellant further submits that "in rejecting claim 9, the Examiner indicated that the memory modules were the equivalent of the target devices; in rejecting claims 10 and 11, the Examiner equated an I/O module 104 and a controller 1920 as being target devices and that one of ordinary

skill in the art would not understand both the memory modules and controllers to be the same as target devices".

Examiner respectfully disagrees. The recitations of "target devices" in claim 1 connote both the idea of having "target devices" of the same type (e.g., plurality of memory modules, **or** I/O controllers, **or** disk array controllers) and the idea that the "target devices" are of different kind (e.g., memory module/s, I/O controller/s, **and** disk array controller/s). It appears that Appellant misunderstood the Examiner's position when it comes to the rejection of claims 5 and 6. Claims 5 and 6, to further limit independent claim 1, recite that the target devices **comprise** input/output controllers or disk array controllers. Note that claims 5 and 6 do not recite that the target devices ***are*** input/output controllers or disk array controllers but "the target devices" **comprise** input/output controllers or disk array controllers. As claimed, claims 5 and 6 do not prevent "the target devices" of claim 1 from being of one type (e.g., the memory modules of Leung) and of a different kind (e.g., input/output controllers and disk array controllers). In view of the foregoing, Leung discloses both "the plurality of target devices" of claim 1 [*plurality of memory arrays*; Fig. 1; col. 3, lines 63-65], and "the target devices comprise input/output controllers and disk array controllers" of claims 5 and 6 [*Fig. 1 shows I/O module 104 which controls the memory devices where one or more master devices can be attached to the I/O bus to control the operations in the system, and Fig. 19 shows a memory controller as that master device; note that Leung discloses one or more master devices control the operation of the system and the master device/s is/are in fact controller/s; hence, one*

more master devices here mean one or more controllers; thus, the plurality of controllers of Leung read on the claims 10 and 11 as the plurality of target devices; col. 25, lines 28-38].

Appellant argues on page 25, with respect to claim 13, that Leung fails to disclose "wherein each of the plurality of groups is associated with a single base memory address".

The combination of Leung and Guttag was relied upon in rejecting the claims. Guttag discloses "each of a plurality of n processors has a predetermined plurality of corresponding memories, wherein the predetermined plurality of memories having a corresponding fixed base address; and a base address instruction executing on any one of the plurality of n processors generating the base address of the predetermined plurality of memories; col. 172, ll 48-60". Furthermore, in col. 5, lines 36-41, Guttag discloses "a plurality of corresponding memories having a unique addressable memory of a single memory space wherein these corresponding memories have a corresponding base address within the single memory address space".

It is worth mentioning that Guttag discloses a one to one correspondence between the "plurality of memories" and the "**a** corresponding fixed base address".

Leung also discloses associating the plurality of target devices with a single base memory address [col.4, lines 31-34]; and executing a memory access using the single base memory address [col.4, lines 44-46]. Furthermore,

Leung discloses the "single base memory" address claimed by Applicant [col.4, lines 20-35; col. 5, lines 5-8] where the base address can be associated with either a single target device or a group of target devices.

Appellant submits on page 26 of the remarks, with respect to claims 16 and 25, that "the I/O module cannot reasonably be considered an initiator and the memory modules cannot reasonably be considered the target devices of claims 16 and 25".

Examiner respectfully disagrees. The reasoning pertaining to claim above applies as well to claims 16 and 25. Claims 16 and 25 simply recite "an initiator device coupled to the bus, the initiator device configured to initiate/issue a (transaction request)/ (multicast transaction)" and Leung clearly discloses [*all memory transactions are initiated by either I/O module 104* ***or*** *by devices connected to I/O bus 106*; col.7, lines 45-46] where it is readily apparent that the transactions are initiated by either the I/O module **or** devices connected to the bus. In this case, either the I/O mode or the other devices connected to the bus can play the role of the "initiator device" broadly claimed.

Appellant further argues on pages 26 and 27, regarding claims 16, 17, 25, and 26, that "Examiner indicated that the I/O module 104 is an initiator in rejecting claims 16 and 25, but in the rejection of claims 17 and 26 indicated that the I/O module 104 is a target device".

Examiner respectfully disagrees. Claims 17 and 26 simply recite "the plurality of target devices comprise input/output controllers". The recitations of "target devices" in claim 1 connote both the idea of having "target devices" of the same type (e.g., plurality of memory modules, **or** I/O controllers, **or** disk array controllers) and the idea that the "target devices" are of different kind (e.g., memory module/s, I/O controller/s, **and** disk array controller/s). It appears that Appellant misunderstood the Examiner's position when it comes to the rejection of claims 5 and 6. Claims 5 and 6, to further limit independent claim 1, recite that the target devices **comprise** input/output controllers or disk array controllers. Note that claims 5 and 6 do not recite that the target devices ***are*** input/output controllers or disk array controllers but "the target devices" **comprise** input/output controllers or disk array controllers. As claimed, claims 5 and 6 do not prevent "the target devices" of claim 1 from being of one type (e.g., the memory modules of Leung) and of a different kind (e.g., input/output controllers and disk array controllers). In view of the foregoing, Leung discloses both "the plurality of target devices" of claim 1 [*plurality of memory arrays*; Fig. 1; col. 3, lines 63-65], and "the target devices comprise input/output controllers and disk array controllers" of claims 5 and 6 [*Fig. 1 shows I/O module 104 which controls the memory devices where one or more master devices can be attached to the I/O bus to control the operations in the system, and Fig. 19 shows a memory controller as that master device; note that Leung discloses one or more master devices control the operation of the system and the master device/s is/are in fact controller/s; hence, one more master devices here mean one or more*

controllers; *thus, the plurality of controllers of Leung read on the claims 5 and 6 as the plurality of target devices*; col. 25, lines 28-38].

Appellant further posits on page 26, paragraph 3, that there is simply nothing in Leung that can reasonably be construed as disclosing "a single base address associated with the plurality of target devices", recited in claims 16 and 25.

The combination of Leung and Guttag was relied upon in rejecting the claims. Guttag discloses "each of a plurality of n processors has a predetermined plurality of corresponding memories, wherein the predetermined plurality of memories have a corresponding fixed base address; and a base address instruction executing on any one of the plurality of n processors generating the base address of the predetermined plurality of memories; col. 172, ll 48-60". Furthermore, in col. 5, lines 36-41, Guttag discloses "a plurality of corresponding memories having a unique addressable memory of a single memory space wherein these corresponding memories have a corresponding base address within the single memory address space".

It is worth mentioning that Guttag discloses a one to one correspondence between the "plurality of memories" and the "**a** corresponding fixed base address".

Leung also discloses associating the plurality of target devices with a single base memory address [col.4, lines 31-34]; and executing a memory access using the single base memory address [col.4, lines 44-46]. Furthermore,

Leung discloses the “single base memory” address claimed by Applicant [col.4, lines 20-35; col. 5, lines 5-8] where the base address can be associated with either a single target device or a group of target devices.

Appellant argues on page 31, paragraph 1, with respect to claim 32, that Gupta does not disclose “a plurality of devices simultaneously accessing associated interleaved memory regions in response to a single transaction”.

The combination of Guttag, Gupta, and Blaner was relied upon in rejecting claim 32. Claim 32 simply requires “a plurality of devices simultaneously accessing associated interleaved memory regions in response to a single transaction”. Gupta discloses [*two or more memory busses can each perform memory transactions simultaneously, with each memory bus coupled to one or more memory bus segments, wherein a single memory transaction can be active on a single memory bus segment at any given time, and each memory bus segment is coupled to one or more interleaved memory banks*; col. 16, ll 15-23].

While Gupta discloses “a plurality of devices simultaneously accessing associated interleaved memory regions”, Blaner further teaches doing so in response to a single transaction [*interleaved memory banks wherein a group of the interleaved memory banks are accessible in parallel in response to a single access*; col. 8, ll 22-26] as claimed.

Appellant assumes on page 31, paragraph 2, that there is nothing in Gupta with respect to “the plurality of devices having a common base address", recited in claim 32.

The combination of Guttag, Gupta, and Blaner was relied upon in rejecting claim 32. Guttag discloses in col. 5, lines 36-41 that "a plurality of corresponding memories having a unique addressable memory of a single memory space wherein these corresponding memories have a corresponding base address within the single memory address space". It is worth mentioning that Guttag discloses a one to one correspondence between the "plurality of memories" and the "**a** corresponding fixed base address".

Appellant argues on pages 31-32, with respect to claim 32, that there is no mention in Blaner of "a plurality of devices having a common base address wherein each simultaneously accesses its associated interleaved memory region in response to a single transaction request directed to the common base address".

The combination of Guttag, Gupta, and Blaner was relied upon in rejecting claim 32. Guttag discloses in col. 5, lines 36-41 that "a plurality of corresponding memories having a unique addressable memory of a single memory space wherein these corresponding memories have a corresponding base address within the single memory address space". It is worth mentioning that Guttag discloses a one to one correspondence between the "plurality of memories" and the "**a** corresponding fixed base address".

Gupta also clearly discloses [*two or more memory busses can each perform memory transactions simultaneously, with each memory bus coupled to one or more memory bus segments, wherein a single memory transaction can be active on a single*

memory bus segment at any given time, and each memory bus segment is coupled to one or more interleaved memory banks; col. 16, ll 15-23].

While Gupta discloses "a plurality of devices simultaneously accessing associated interleaved memory regions", Blaner further teaches doing so in response to a single transaction [*interleaved memory banks wherein a group of the interleaved memory banks are accessible in parallel in response to a single access*; col. 8, ll 22-26] as claimed.

Appellant argues on page 33, paragraph 2, with respect to claim 47, that Guttag does not disclose assigning a common base address to a plurality of disk drives".

Guttag discloses in col. 5, lines 36-41 that "a plurality of corresponding memories having a unique addressable memory of a single memory space wherein these corresponding memories have a corresponding base address within the single memory address space". It is worth mentioning that Guttag discloses a one to one correspondence between the "plurality of memories" and the "**a** corresponding fixed base address".

Appellant argues on page 34, paragraph 3, with respect to claim 47, that Gupta does not disclose "assigning a portion of data storage to each disk drive of the collective target group".

Gupta discloses assigning a portion of data storage to each disk drive of the collective target group [Figs. 1-2; col. 1, lines 37-64; *memory array with multiple*

banks of rows and columns divided into different arrays of memory or banks that can operate independently; col. 2, lines 55-60; col. 16, lines 15-23].

Appellant argues on page 37, with respect to claims 33 and 36, that Gupta does not disclose that "the same single base memory address is associated with each of a plurality of target devices".

Claims 33 and 36 are rejected over the combination of Leung, Guttag, and Gupta.

Guttag discloses "each of a plurality of n processors has a predetermined plurality of corresponding memories, wherein the predetermined plurality of memories have a corresponding fixed base address; and a base address instruction executing on any one of the plurality of n processors generating the base address of the predetermined plurality of memories corresponding to the one processor; col. 172, ll 48-60". Furthermore, it is abundantly clear in col. 5, lines 36-41 that Guttag discloses "a plurality of corresponding memories having a unique addressable memory of a single memory space wherein these corresponding memories have a corresponding base address within the single memory address space".

It is worth mentioning that Guttag discloses a one to one correspondence between the "plurality of memories" and the "**a** corresponding fixed base address" in contrast to applicant's representative assertion.

Leung also discloses associating the plurality of target devices with a single base memory address [col.4, lines 31-34]; and executing a memory access using the single base memory address [col.4, lines 44-46]. Furthermore, Leung discloses the "single base memory" address claimed by Applicant [col.4, lines 30-35] where the base address can be associated with either a single target device or a group of target devices.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Mardochee Chery/
Examiner

Conferees:

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12/03/08

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